Remarks

Reconsideration and allowance of the subject patent application are respectfully requested.

Claims 1-9, 11-14 and 16-32[1] were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by Hsu et al. (U.S. Patent No. 5,754,647).

The office action contains various references "Takata" in connection with the rejections. The undersigned confirmed with the Examiner that these are typographical errors and the references should be to "Hsu et al."

The software protection apparatus of Hsu et al. is based on an assumption that certain addresses of a memory storing a game program are not accessed during normal game operation. See Hsu et al., col. 5, line 62 to col. 6, line 2 ("A typical game machine does not access the entire address space of its memory, and in fact, software programs may be designed to intentionally avoid access of certain designated address locations. In other words, the address locations that are intentionally not used will never be accessed by the CPU 14 of the game machine system during normal operation of the system, and these addresses should never appear on the address bus 20.") However, potential infringers of the software program would not know these addresses and thus an emulator designed by such infringers would access these addresses. Consequently, Hsu et al. describes a trap address detector that detects when such "illegal" addresses are accessed. As a result of detecting these addresses, "the data read out of the inconsistent memory device 32 is erroneous for a continuous block of data accessed. The size of this block of data may be predetermined, or it may be the same size as the block of data defined by the illegal addresses accessed." Col. 6, lines 22-26.

Applicants find no disclosure of, for example, methods and devices as in, for example, claims 1, 7, 8, 9 and 14 which involve a first store and a second store and the enabling/disabling of reading from these stores depending on an input address. The disclosure at col. 5, line 59 to col. 6, line 46 of Hsu et al., which is referenced in connection with each and every limitation of

[1] Applicants believe claim 2 should be omitted from the listing of claims because claim 2 is elsewhere rejected as allegedly being "obvious" over Hsu et al.

independent claims 1, 7, 8, 9 and 14[2], does not disclose (and is not suggestive of) first and second stores (or storage areas) each of which stores portions of "regular data" (or an application program or a game program). In Hsu et al., the data is not arranged in first and second stores (or storage areas) as claimed and the detection of addresses for "trap" locations simply causes an "erroneous data dump." See col. 5, line 26.

Consequently, Applicants respectfully submit that Hsu et al. does not anticipate claims 1, 7, 8, 9 and 14.

Independent claims 19 and 28 each calls for a video game program memory and a memory separate from the video game program memory. A first part of a video program and dummy data are stored in the video game program memory and a second part of the video game program is stored in the separate memory. As noted above, Hsu et al. discloses the outputting of erroneous data when certain memory addresses are "trapped." Hsu et al. does not disclose memories arranged in the manner specified in these claims. Consequently, Applicants respectfully submit that Hsu et al. does not anticipate claims 19 and 28.

The claims that depend from claims 1, 7, 8, 9, 14, 19 and 28 are not anticipated by Hsu et al. because of these dependencies and because of the additional patentable features contained therein.

By way of example without limitation, the office action references col. 6, lines 55-67 of Hsu et al. in connection with the feature of claim 4 in which the nonvolatile semiconductor memory is constructed such that data is written with a first write voltage in the second regular data storing area and the dummy address storing area, and data is written with a second write voltage lower than the first write voltage in other areas. However, the referenced portion of Hsu et al. describes a design for implementing the "interference method of software protection" (see col. 7, lines 1-3) and provides no disclosure with respect to first and second write voltages as claimed.

Similarly, col. 6, lines 55-67 of Hsu et al. do not disclose or suggest the first and second write voltages of claims 12, 17, 24-27 and 29-32.

Claims 2, 10 and 15 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Hsu et al. Even assuming for the sake of argument that the provision of a mask

[2] Claims 19-27 and 28-32 are rejected by analogy to other claims.

ROM and a non-volatile memory as specified in these claims would have been obvious, Hsu et al. nonetheless remains deficient with respect to the claims from which claims 2, 10 and 15 depend.

For at least the reasons set forth above, the pending claims are believed to be allowable and favorable office action is respectfully requested. Should the Examiner believe that further discussion would be helpful to advance prosecution, he is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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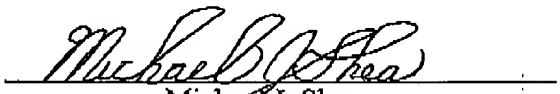
By: 
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